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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,609	05/31/2001	Bret Ronald Olszewski	AUS920000844US1	1789

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EXAMINER	
VO, LILIAN	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,609	OLSZEWSKI ET AL.	
	Examiner	Art Unit	
	Lilian Vo	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 23 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 12 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar et al. (US 6,058,466, hereinafter Panwar).

4. Regarding **claims 1, 12 and 23**, Panwar discloses:

a multiprocessor system with many execution resources may be sharing among multiple logical processors on a single integrated circuit chip (col. 5, lines 23 – 26);

determining whether a first logical processor on the first physical processor is idle (col. 8, lines 10 - 13);

determining whether a second logical processor on the first physical processor is busy if the first logical processor is idle (col. 8, lines 11 – 22, col. 15, line 63 – col. 16, line 5); and

relinquishing resources of the first physical processor to the second logical processor if the second logical processor is busy (col. 8, lines 15 – 22, col. 15, line 63 – col. 16, line 5).

With respect to the steps of determining whether a second logical processor on the first physical processor is busy if the first logical processor is idle and relinquishing resources of the first physical processor to the second logical processor if the second logical processor is busy, Panwar discloses that each virtual processor in the active state is assigned exclusive control over some of the shared resources in the functional units of processor 102 (col. 7, lines 54 – 56) and that when a napping virtual processor encounters a cache miss that must be satisfied by main memory …, the virtual processor enters the sleep state (col. 8, lines 11 – 13). During the sleeping state, the virtual processor not only preventing from taking additional resources but it also forced to release resources previously occupied so that other virtual processors may continue execution unimpaired …(col. 8, lines 15 – 22). By removing these instructions, pickers 802a and 802b can move forward to pick instructions from active processes (col. 15, line 63 – col. 16, line 5). In other words, if the system detects any virtual processor is being idle, the virtual processor allocated resources are to be released (deallocated) for use by other active processes in other virtual processor. Hence, it would have been obvious for one of an ordinary skill in the art, to recognize that virtual processors are being monitored to determined if they are in the active (busy) state or in an inactive (idle) state in order for the system to know to release shared resources from the idle virtual processor and allocated them to other busy virtual processors.

5. Claims 2 - 6 and 13 - 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar et al. (US 6,058,466), as applied to claims 1, 12 and 23 above, in view of applicants' admitted prior art (hereinafter AAPA).

6. Regarding **claim 2**, Panwar discloses the step of detecting the first logical processor is idle by determining that the first logical processor is not currently running a job (col. 8, lines 11 – 22, col. 15, line 63 – col. 16, line 5). Panwar however did not clearly disclose the additional limitation as claimed. Nevertheless, the concept of recognizing that the run queue associated with a processor is empty if the processor is not currently running a job, is considered well known and also disclosed in AAPA in specification page 3, lines 11 – 13 (when a logical processor becomes idle and there are no threads waiting in the run queue...). It would have been obvious to one of an ordinary skill in the art, at the time of the invention to incorporate AAPA's teaching to the system of Panwar so that the idle processor can affectively utilize the resources by stealing or acquiring threads from another logical processor's run queue (AAPA: specification 3, lines 15 – 16).

7. Regarding **claims 3 and 4**, as modified Panwar discloses the concept of when a logical processor becomes idle and there is no threads waiting in the run queue, the processor checks for threads to acquire from another processor's run queue (AAPA: specification page 3, lines 11 – 15). It is obvious to one of an ordinary skill in the art, at the time the invention was made, to recognize that if there is any thread waiting in the run queue (not empty), the processor would process it first before consider stealing or acquiring threads from the other processor. As a result, the run queue is not empty if there is thread waiting and by processing the thread, the processor is busy, not idle.

8. Regarding **claims 5 and 6**, as modified Panwar discloses the concept of when a logical processor becomes idle and there is no threads waiting in the run queue, the processor checks for threads to acquire from another processor's run queue and that moving a thread between physical processors is expensive (AAPA: specification page 3, lines 11 – 18). It is obvious to one of an ordinary skill in the art, at the time the invention was made, to recognize that the concept of checking for threads from another processor's run queue also mean a run queue corresponding to a different physical processor as well. As a result, if there is any thread available (waiting) from another run queue, it will be acquired and processed.

9. **Claims 13 – 17** are rejected on the same ground as stated in claims 2 – 6 above.

10. Claims 7, 8 and 18 - 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar et al. (US 6,058,466), as applied to claims 1, 12 and 23 above, in view of AAPA, and further in view of Koning (US Pat. Application Publication 2002/0133530).

11. Regarding **claims 7 and 8**, as modified Panwar discloses that one of the logical processors consumes resources of the physical processor (AAPA: specification page 2, lines 6 – 8: when a thread is dispatched to a logical processor, the thread runs as if it is the only thread running on the physical processor). As modified Panwar did not clearly specify that the other logical processor, which relinquished resource, is having a lower priority. Nevertheless, Koning discloses that when a higher priority task (in the 2nd logical processor) that is ready to run, it preempts a currently running lower priority task (in the 1st logical processor) (page 7, paragraph

0087). Thus, when the currently running task (in the 1st logical processor) gives up its resource to a higher priority task (in the 2nd logical processor), the logical processor, which runs the current task, is lowering its priority. It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to incorporate this concept to Panwar and AAPA to allow a higher priority task to preempt the lower priority task until its priority is lower (Koning: page 1, paragraph 0004).

12. **Claims 18 – 19** are rejected on the same ground as stated in claims 7 – 8 above.

13. Claims 9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar et al. (US 6,058,466), as applied to claims 1, 12 and 23 above, in view of AAPA, in view of Koning (US Pat. Application Publication 2002/0133530), and further in view of Welland et al. (US 5,247,677, hereinafter Welland).

14. Regarding **claim 9**, as modified Panwar did not disclose the additional limitation as claimed. Nevertheless, Welland discloses the concept of lowering the priority of the logical processor for a predetermined time period (col. 4, line 62 – col. 5, line 17: task 24c current priority is raised from 12 to 15 making task 24c the highest priority which is to be scheduled for execution and at the end of one time slice, the current priority of task 24c would be decremented). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to incorporate this concept to modified Panwar to take an advantage of new

priority based scheduling process that does not allow lockout to occur so that all tasks will get to run, even the low priority tasks (Welland: col. 1, lines 41 – 51).

15. **Claim 20** is rejected on the same ground as stated in claim 9 above.

16. Claims 10, 11, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar et al. (US 6,058,466), as applied to claims 1, 12 and 23 above, in view of AAPA, in view of Koning (US Pat. Application Publication 2002/0133530), in view of Welland et al. (US 5,247,677) and further in view of Kimmel et al. (6,105,053, hereinafter Kimmel).

17. Regarding **claim 10**, as modified Panwar did not clearly disclose the additional limitation as claimed. Nevertheless, Kimmel discloses the concept of raising the priority of a processor after a predetermined time period (col. 14, lines 10 – 15). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to incorporate Kimmel's teaching to modified Panwar so that a thread group that is queued but not executed for a time period can be serviced accordingly (Kimmel: col. 14, lines 10 – 22).

18. Regarding **claim 11**, as modified Panwar discloses the concept of dispatching a job to the logical processor in response to the raised priority (col. 14, lines 18 – 22, 28 - 36).

19. **Claims 21 and 22** are rejected on the same ground as stated in claims 10 - 11 above.

Response to Arguments

20. Applicant's arguments filed 6/1/05 have been fully considered but they are not persuasive for the reasons set forth below.

21. Regarding applicant's argument that Panwar does not teach any type of determination of whether a processor is busy or idle (page 6, 5th paragraph), the examiner disagrees. Panwar discloses when a virtual processor encounters a cache miss, the virtual processor enters the sleep state (col. 8, lines 10 – 13) and the sleeping processor is prevented from taking additional resources, but it is also forced to release resources previously occupied so that other virtual processors may continue execution unimpaired (col. 8, lines 13 – 22). In other words, when the virtual processor enters the sleep state, the virtual processor becomes idle and is forced to release any resource that it's been occupied to other active (busy) virtual processors. It is obvious from this that Panwar has to determine a processor state to know if it is in active or idle. If there is no determination process in Panwar, then how can Panwar know that the processor is in a sleep or active state? Also, claim language does not require the processor to perform certain function and/or meet certain condition to be in an idle state. Therefore, the cited reference meets the claim and this argument is moot.

22. Regarding applicant's argument that Panwar does not teach or suggest a conditional relinquishment of resource based upon whether the second logical processor is busy (page 7, 1st paragraph), the examiner disagrees.

Panwar discloses that each virtual processor in the active state is assigned exclusive control over some of the shared resources in the functional units of processor 102 (col. 7, lines 54 – 56) and that when a napping virtual processor encounters a cache miss that must be satisfied by main memory …, the virtual processor enters the sleep state (col. 8, lines 11 – 13). During the sleeping state, the virtual processor not only preventing from taking additional resources but it also forced to release resources previously occupied so that other virtual processors may continue execution unimpaired …(col. 8, lines 15 – 22). By removing these instructions, pickers 802a and 802b can move forward to pick instructions from active processes (col. 15, line 63 – col. 16, line 5). In other words, if the system detects any virtual processor is being idle, the idle virtual processor resources are to be released (deallocated) for use by other active processes in other virtual processors. Hence, it would have been obvious for one of an ordinary skill in the art, to recognize that virtual processors are being monitored to determined if they are in the active (busy) state or in an inactive (idle) state in order for the system to know when to release shared resources from the virtual processor when it becomes idle and allocated the resource to other busy virtual processors.

The claim language requires that the relinquishment of resources to the busy logical processor. Panwar clearly states that the resource is released for use by other active virtual processors. Furthermore, applicant is claiming to release the resource to the busy processor from the idle processor only if there exists an idle processor. In other words, according to applicant's invention, if the first logical processor is not idle and the second logical processor is determined to be busy, meaning both logical processors are concurrently busy, there would NOT be any relinquishment of resources. Therefore, the cited Panwar read on the claimed invention.

With respect to applicant's remark that "the cited reference merely states that the sleeping processor is unconditionally prevented from taking additional resources and release resources previously provided" (page 7, 1st paragraph), this cited passage means that idle processor cannot take any resource and at the same time has to release any resources that it is currently holding for use by other active processors (busy processors).

23. Regarding applicant's remark that AAPA page 3, lines 11 – 13 "does not establish that it was well-known to perform a conditional determining step..." (page 8, 1st paragraph), the examiner clearly stated in the office action that it is the concept of recognizing that the run queue associated with a processor is empty if the processor is not currently running a job (idle) because there are no threads waiting in the run queue, is considered well known as stated in AAPA that when a logical processor becomes idle and there are no threads waiting in the run queue. AAPA also discloses that the processor checks for threads to steal or acquire from another logical processor's run queue (page 3, lines 13 – 15). By deciding to steal threads from other run queue, it must have determined that its queue is empty. Otherwise, the processor would not need to steal threads and just execute threads from its own queue. It is a common sense for a processor to steal thread when it does not have any threads in its queue, thus having an empty queue. Therefore, it is considered well know and obvious to recognize that the run queue associated with a processor is empty if the processor is not currently running a job when it decide to steal threads from another run queue.

24. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning (page 9, 1st paragraph), it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

25. In response to applicant's argument that Panwar reference are specifically directed to reacting to a cache miss event to trigger association actions (page 9, 1st paragraph), the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

26. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, the motivation for the rejection is found in the reference (AAPA specification page 3, lines 15 – 16).

27. Regarding applicant's allegation that Panwar teach away from the features of claim 5 (page 11, 1st paragraph), Panwar does not teach away from the feature of claim 5 because of technical issues pertinent to the disclosed invention, but rather discloses a multiprocessor system with many execution resources may be sharing among multiple logical processors on a single integrated circuit chip (col. 5, lines 23 – 26).

Furthermore, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

28. Regarding applicant's argument that Koning's scheduler is not in any way involved with changing or modifying priorities of tasks (page 11, 5th paragraph), applicant is arguing a feature that is not specifically stated in the claim language, which is improper. Claim 8 recites the limitation of lowering the priority of the logical processor (logical context) not of the tasks by relinquishing the physical resource. By this, it means that the logical processor yields the processor to the other active/busy logical processor. Koning discloses that when a higher priority task (in 2nd logical processor) that is ready to run, it preempts a currently running lower priority task (in 1st logical processor) (page 7, paragraph 0087). Thus, when the currently running task (in 1st logical processor) gives up its resource to a higher priority task (in the 2nd logical

processor), the logical processor (context), which runs the current task, is lowering its priority. It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to incorporate this concept to Panwar and AAPA to allow a higher priority task to preempt the lower priority task until its priority is lower (Koning: page 1, paragraph 0004).

29. Applicant's arguments with respect to claims 9, 10, 11, 20, 21 and 22 (page 12, 1st – 2nd paragraphs) fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Conclusion

30. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Monday - Thursday, 7:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist at 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo
Examiner
Art Unit 2195

lv
August 11, 2005

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